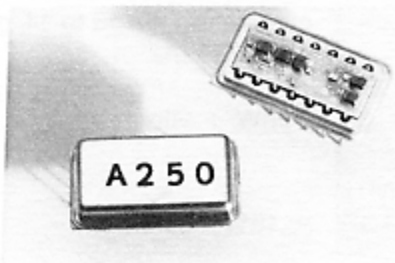
# CHARGE SENSITIVE PREAMPLIFIER

# A250

## A NEW STATE-OF-THE-ART




- External FET allows matching to detector
- FET can be cooled
- Noise at room temperature ≅100 electrons RMS
- Low power (19 mW typical)

The A250 is a hybrid state-of-the-art Charge Sensitive Preamplifier for use with a wide range of detectors with capacitance from <1 to several thousand picofarads. Such detectors include silicon, CdTe and $HgI_2$ solid state detectors, proportional counters, photomultiplier tubes, piezoelectric devices, photodiodes, CCD's and others.

To permit optimization for a wide range of applications, the input field effect transistor is external to the package and user selectable. This feature is essential in applications where detector and FET must be cooled to reduce noise. In all applications it allows the FET to be matched to the particular detector capacitance, as well as to noise and shaping requirements. In larger quantities, the A250 may be special ordered with internal FET.

The noise performance of the A250 is such that its contribution to FET and detector noise is negligible in all charge amplifier applications, i.e., it is essentially an ideal amplifier in this respect.

The internal feedback components configure the A250 as a charge amplifier; however, it may be used as a high performance current or voltage preamplifier by choice of suitable feedback components.

While these preamps were designed for multidetector satellite instrumentation, their unique characteristics make them equally useful in a broad range of laboratory and commercial applications.

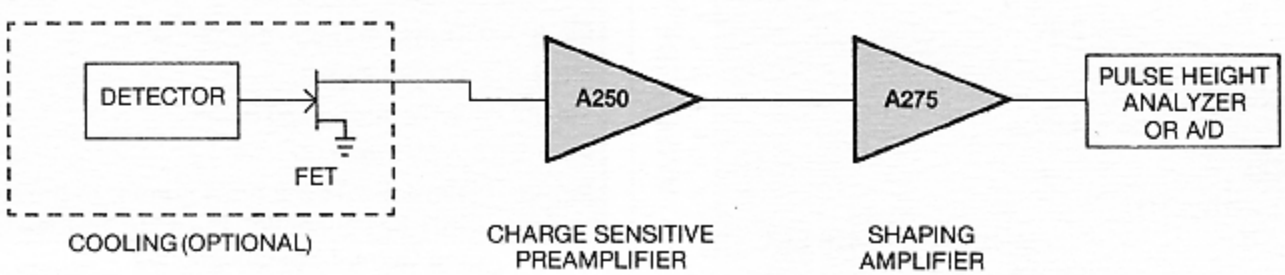
### FEATURES

- Ultra low noise
- Low power
- Fast rise time (4ns at 0pf)
- External FET (allows selection or cooling)
- Positive or negative signal processing
- Pin selectable gain
- Small size (14 pin hybrid DIP)
- High reliability screening
- One year warranty

### APPLICATIONS

- Aerospace
- Nuclear physics
- Portable instrumentation
- Nuclear monitoring
- Particle, $\gamma$ and X-ray imaging
- Medical and nuclear electronics
- Electro-optical systems

### TYPICAL APPLICATION




AMPTEK INC. 6 DE ANGELO DRIVE, BEDFORD, MA 01730 U.S.A. TEL. (781) 275-2242 FAX: (781) 275-3470
email: sales@amptek.com www.amptek.com

# SPECIFICATIONS

($V_S = \pm 6V$, $T = 25°C$) unloaded output

## INPUT CHARACTERISTICS

| | |
|---|---|
| SENSITIVITY ($C_f = 1pF$): | 44 mV/Mev (Si)<br>55 mV/Mev (Ge)<br>36 mV/Mev (CdTe)<br>38 mV/Mev ($HgI_2$)<br>1V/pC<br>0.16 $\mu$V/electron |

Sensitivity can be reduced by connecting PINS 2 and/or 3 to PIN 1 thus providing $C_f = 3$, 5 or 7 pF. Additional external capacitors can be added for further reduction of gain. In general, the sensitivity is given by $A = 1/C_f$ (pF) V/pC. For Silicon the sensitivity is $A = 44/C_f$ (pF) mV/Mev.

| | |
|---|---|
| NOISE: | Input FET dependent. See Figure 1. |
| NOISE SLOPE: | Input FET dependent. See Figure 1. |

Data presented in Figure 1 is representative of results obtained with recommended FETs, and is characteristic of the FET and shaping time constants rather than the A250, which is effectively noiseless. In general, the choice of input FET is based on its noise voltage specification ($nV/\sqrt{Hz}$) and its input capacitance ($C_{iss}$).

For low capacitance detectors an FET with small $C_{iss}$ should be chosen, such as 2N4416 or 2SK152.

For very high capacitance detectors, two or more matched high $C_{iss}$ FETs such as the 2N6550 may be paralleled to achieve the best noise performance.

| | |
|---|---|
| DYNAMIC INPUT CAPACITANCE: | > 40,000 pF with 2X2SK147 FETS and $C_f = 5pF$ |
| POLARITY: | Negative or Positive |

## OUTPUT CHARACTERISTICS

| | |
|---|---|
| POLARITY: | Inverse of input |
| RISE TIME: | 3.8ns at 0pF input load with 2SK152<br>4.5ns at 100pF input load with 2N6550 or 2SK152<br>Figure 2, Figure 3 |
| OUTPUT IMPEDANCE: | 100 Ohms |
| INTEGRAL NONLINEARITY: | < .03% for 0 to + 2V unloaded<br>< .006% for 0 to − 2V unloaded |
| DECAY TIME CONSTANT: | 300 Mohms $XC_f = 300\mu s$, $900\mu s$, 1.5ms, 2.1ms |
| POSITIVE CLIPPING LEVEL: | > + 2.8V |
| NEGATIVE CLIPPING LEVEL: | < − 4.6V |

## GENERAL

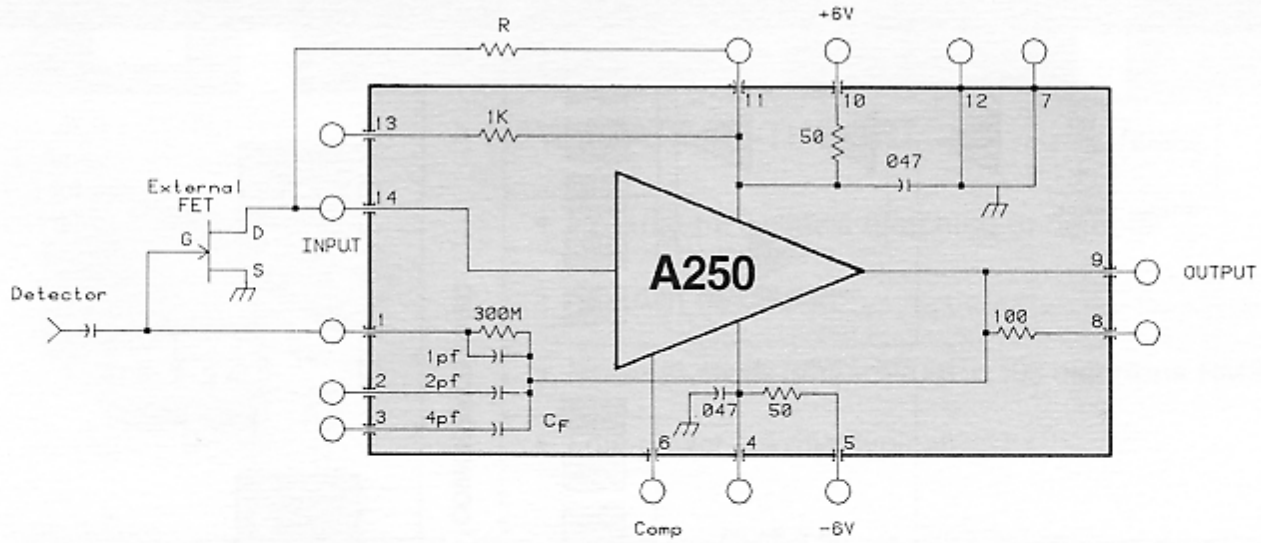
| | |
|---|---|
| GAIN-BANDWIDTH PRODUCT: | $f_T > 300$ MHz with 2N4416 FET —Figure 4.<br>$f_T > 1.5$ GHz with two 2SK147 FETs—Figure 4. |
| OPERATING VOLTAGE: | ± 6V, (± 8V Maximum) |
| OPERATING CURRENT: | ± 1.2 ma plus the FET drain current ($I_{DS}$). Where: $I_{DS}$ (ma) = 3/R(KΩ) − 0.25. As a special case, the internal 1K resistor may be used for R, by connecting Pin 13 to 14, giving $I_{DS} = 2.75$ ma. |
| POWER DISSIPATION: | $14mW + 6[I_{DS}]$ |
| VARIATION OF SENSITIVITY WITH SUPPLY VOLTAGE: | < .15%/V at ± 6V |
| TEMPERATURE STABILITY: | < .1% from 0° to + 100°C<br>< .5% from − 55°C to + 125°C |
| OPERATING TEMPERATURE: | − 55° to + 125°C |
| STORAGE TEMPERATURE: | − 65°C to + 150°C |
| SCREENING: | AMPTEK HIGH RELIABILITY |
| PACKAGE: | 14 PIN Hybrid DIP (Metal) |
| WARRANTY: | One year |
| TEST BOARD: | PC-250 |
| OPTIONS: | — Internal FET (consult factory)<br>— NASA GSFC S-311-P-698 screening |

## PIN CONFIGURATION

(14 Pin Hybrid DIP)

| | |
|---|---|
| Pin 1 | 300 Mohm resistor in parallel with 1pF feedback capacitor. Connect this pin to the detector and the Gate of the FET. |
| Pin 2 | 2pF feedback tap. |
| Pin 3 | 4pF feedback tap. |
| Pin 4 | − 6V direct. |
| Pin 5 | − 6V through 50 ohm. |
| Pin 6 | Compensation (0-30pF to ground) for low closed loop gain configuration (where a large feedback capacitor is used together with small detector capacitance). |
| Pin 7, 12 | Ground and case. |
| Pin 8 | Output through 100 ohms. |
| Pin 9 | Output (direct). |
| Pin 10 | + 6V through 50 ohms. |
| Pin 11 | + 6V direct. |
| Pin 13 | Provide 2.75 ma drain current to the external FET by connecting Pin 13 to 14. (See Operating Current Specifications.) |
| Pin 14 | Input. Should be connected to the drain of the FET. This pin is held internally at + 3 Volts. |

## A250 CONNECTION DIAGRAM




## A250 NOISE CHARACTERISTICS

AS A FUNCTION OF DETECTOR CAPACITANCE
INPUT FET, FEEDBACK CAP. AND
SHAPING TIMES
(FET/$I_{DS}$/FEEDBACK CAP./SHAPING TIME)

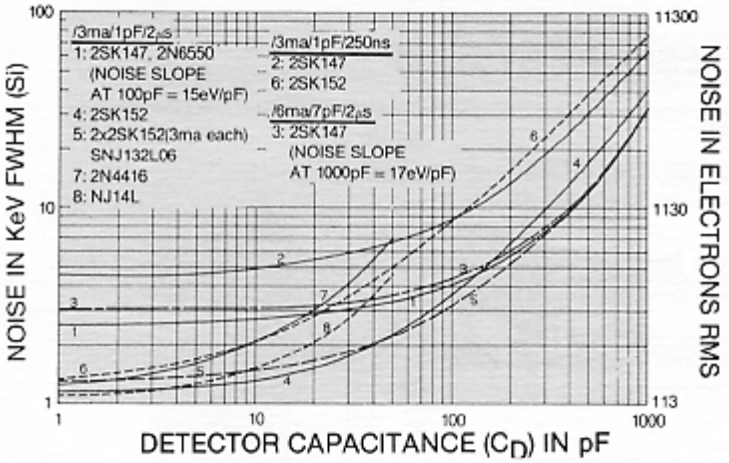



FIGURE 1

## A250 RISE TIME

Vs DETECTOR CAPACITANCE AND FETs

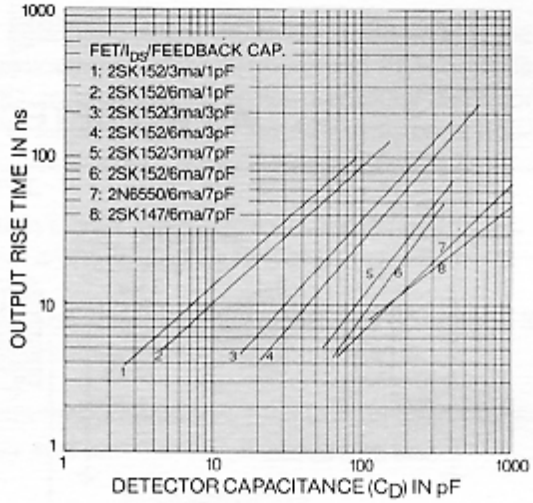
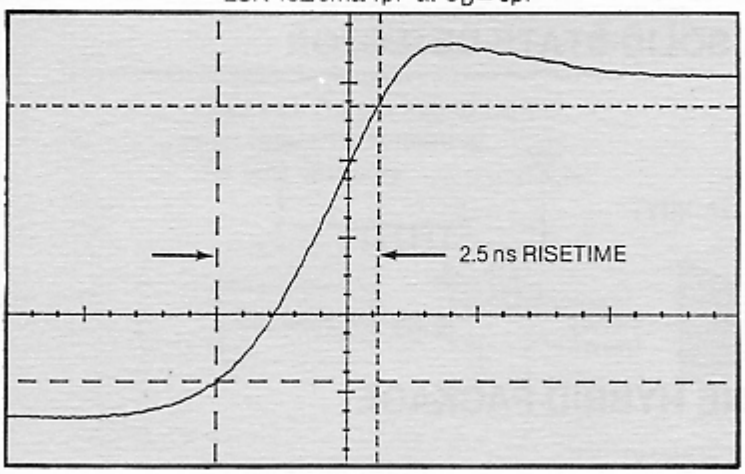



FIGURE 2

## A250 OUTPUT RISETIME

2SK 152/3ma/1pF at $C_D$ = 0pF




Horizontal = 2 ns/div. Vertical = 500 mV/div.
RISETIME = 2.5 ns

FIGURE 3

## A250 SMALL SIGNAL PHASE AND AMPLITUDE Vs FREQUENCY

FOR LOW CAPACITANCE FET: 2N4416(Ciss = 4pF/$I_{DS}$ = 3ma)
FOR HIGH CAPACITANCE FET: 2x2SK147(Ciss = 180pF/$I_{DS}$ = 1.5ma each)

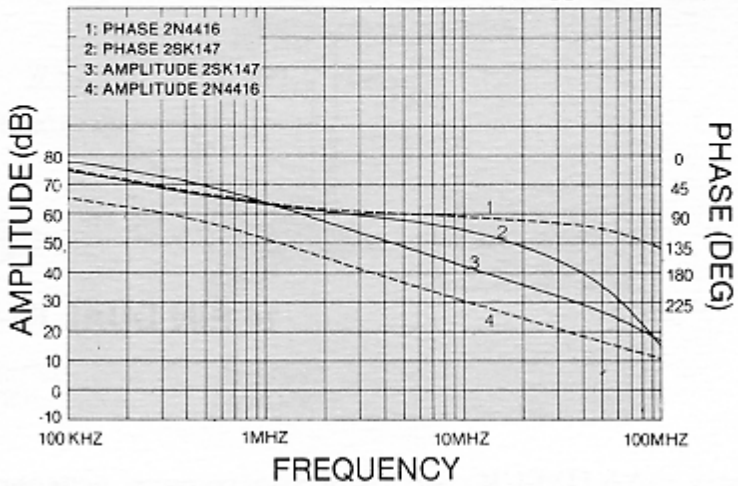
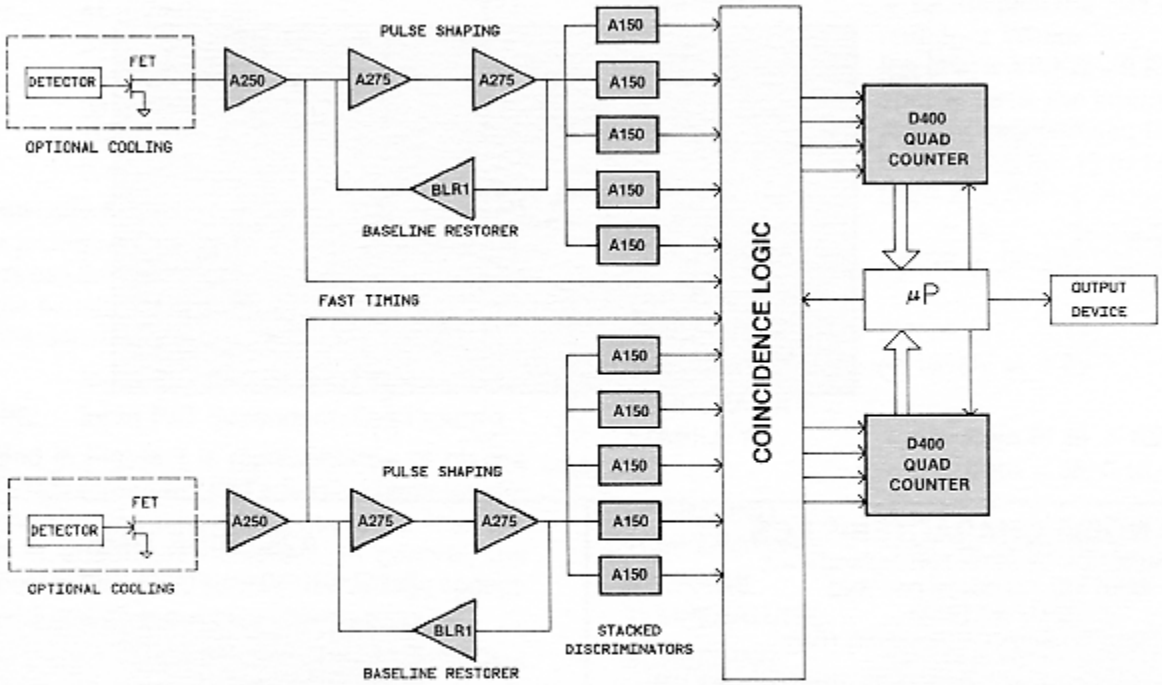
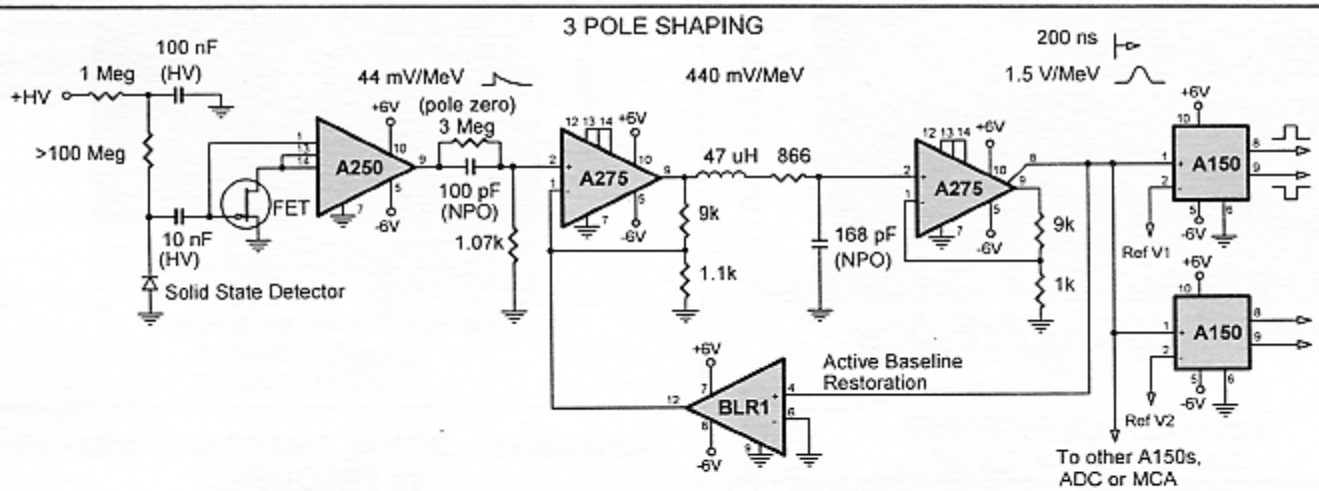



FIGURE 4

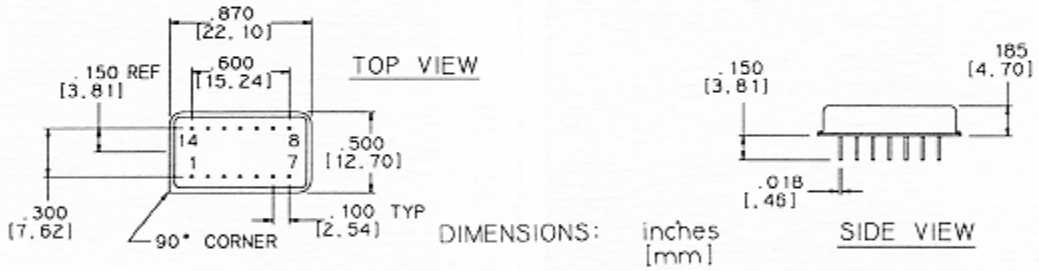
# APPLICATION NOTES




## A TWO DETECTOR TELESCOPE SYSTEM




## THE A250 CONNECTED TO A SOLID STATE DETECTOR




## 14 PIN DUAL IN-LINE HYBRID PACKAGE

AMPTEK INC. 6 DE ANGELO DRIVE, BEDFORD, MA 01730 U.S.A. TEL. (781) 275-2242 FAX: (781) 275-3470
email: sales@amptek.com www.amptek.com